Customer No.: 31561
Docket No.: 13353-US-PA
Application No.: 10/709823

REMARKS

Present Status of the Application

Claims 1-9 are still pending of which the claims 1-3, 6 and 8-9 have been amended and the claim 5 has been canceled without prejudice or disclaimer in order to more explicitly describe the claimed invention. However, applicant respectfully traverses the preceding rejection based on the following arguments. For at least the foregoing reasons, applicants respectfully submit that claims 1-4 and 6-9 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion for amendments to specification

As the Examiner suggest "internal data bus" as claimed in claim 2 be replaced with"internal bus " and reference numerals 31, 51 shown in Fig.3 and 5 represent two independent buses, reference numerals 31, 51 are renamed "a first internal bus" and "a second internal bus," respectively. Accordingly, this amendment doesn't introduce any new matter.

Discussion for title of the invention:

2. The bracket in the title needs to be removed.

In response thereto, applicants request the bracket in the title be removed, and the title is read as:

Customer No.: 31561
Docket No.: 13353-US-PA
Application No.: 10/709823

Discussion for objection to claims 1, 3-4

3. Claims 1, 3, 5, 8, 9 are objected due to their informalities.

In response thereto, claims 1, 3, 8, 9 are amended as instructed as the Examiner, in which claim 5 is merged into the claim 1. Please note that contents of merged claim 5 are also amended in accordance with the Examiner's instruction.

Discussion for objection to claims under 35 U. S. C. 112, 1st paragraph

5. Claims 2-4 are rejected under 35 U. S. C. 112, 1st paragraph, as failing to comply with enablement requirement. The Examiner notes that section [0027] cited by applicant doesn't support data out latch latching control signal.

In re claim 2, the limitation, "a control signal latch coupled to the bus interface unit via the internal data bus, wherein the **data output** latch is a latch for latching a control signal transmitted from the nonreal-time data interface unit to other units," is amended to "a control signal latch coupled to the bus interface unit via the internal data bus, wherein the **control signal** latch is a latch for latching a control signal transmitted from the nonreal-time data interface unit to other units." This amendment is supported in paragraph [0027], part of which is recited as follows:

[0027] In addition, the internal control signal of the nonreal-time data interface unit 210 and the control signal of other functional block of the present invention **are cached in a control signal latch 307** via the internal data bus 31. Then, the control signal for controlling other functional block of the present invention is propagated via a control bus.

6. In claim 5, recitation "the control logic unit controls the data output latch to latch the nonreal-time data, and determines whether to output the nonreal-time data from the data output latch" cannot practice.

In response thereto, from Fig.4, it is obvious for the artisan that once the data output latch 415 extracts the nonreal-time data from the bi-directional bus 41, and the control logic unit 411 controls the data output latch 415 **when** to output the nonreal-time data via the data output bus, not **whether to** output the nonreal-time data because the latched nonreal-time data must be output in accordance with control of the control logic unit 411. Thus, recitation, "and determines **whether to** output the nonreal-time data" in claim 5 is amended to "and determines **when** output the nonreal-time data." Please note that claim 5 is merged to claim 1.

7. Claim 9 recites "the condition selector, coupled to the sequencer, for caching the external condition". One skill in the art would expect a device to catch the data, but not to catch a condition.

In response thereto, lines 8-9 in paragraph [0036] discloses "the external condition is generated by a condition selector which is coupled to the sequencer 603." Thus, the aforementioned recitation in claim 9 is amended to "the condition selector, coupled to the sequencer, for **generating** the external condition" in order to overcome aforementioned rejection.

Discussion for objection to claims under 35 U. S. C. 112, 2nd paragraph

9. Claims 2-5, 9 are rejected under 35 U. S. C. 112, 2nd paragraph as being indefinitely for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In re claim 2, as the Examiner suggest "internal data bus" as claimed in claim 2 be replaced with "internal bus " and reference numerals 31, 51 shown in Fig.3 and 5 represent two independent buses, reference numerals 31, 51 are renamed "a first internal bus" and "a second internal bus," respectively. Therefore, terms "internal data bus" as claimed in claim 2 and claim 6 (i.e. corresponding to reference numeral 51) are amended to "first internal bus" and "second internal bus," respectively.

In re claim 5, please note in previous amended claim 5, the word "the" in recitation "the data output from the I/O unit" is deleted.

In re claim 9, the Examiner rejects the phrase "its determining" because it has no

antecedent. Thus, applicants delete recitation "which is used by the sequencer for its determining" because this recitation is a repeated statement of limitation "sequencer, adjusting a running order according to an external condition."

Discussion for rejection to claims under 35 U. S. C. 103(a)

11. Claims 1, 6-7 are rejected under 35 U.S. C. 103(a) as being unpatentable over Sparr et al. (US 2002/0176390A1).

In response thereto, applicants respectfully traverses the preceding rejection based on the following arguments. To establish a prima facie case of obviousness, **the prior art reference (or references when combined) must teach or suggest all the claim limitations**. The claim 1 is so amended to incorporate claim 5, and the amended claim 1 is partly recited as follows.

1. A real-time data transmission interface comprising:

a nonreal-time data interface unit;

an I/O unit;

a memory unit; and

a network interface control unit;

wherein the I/O unit comprises:

a control logic unit for controlling the I/O unit to perform an input/output operation according to an external control signal;

a checking circuit coupled to the control logic unit, wherein when a self test mode is activated, the control logic unit controls the checking circuit to check an accuracy of data output from the I/O unit and to generate a checking result;

a data output latch coupled to the control logic unit, wherein when the nonreal-time data is transmitted via the I/O unit, the control logic unit controls the data output latch to latch the nonreal-time data, and determines when to output the nonreal-time data from the data output latch; and

a data input latch coupled to the control logic unit, wherein when the real-time data is read via the I/O unit, the data input latch receives the real-time data.

The Examiner alleged that Fig.5, in Sparr, "connection and ports from bus interface 251 and FIFO 295" is identical to claimed I/O unit. However, the claimed I/O unit comprises "**a control logic unit,**" "**a checking circuit,**" "**a data output latch**" and "**a data input latch,**" and these elements are not disclosed in the alleged I/O unit by the Examiner. Furthermore, the rest of Sparr also fails to disclose these elements. Thus, Sparr is not rendered obvious by replacement the real-time transmission interface of Sparr with a radar system, and accordingly patentable.

In re claim 6, applicant respectfully submits that in Fig.5, in Sparr, there only discloses only one address counter and one buffer latch unit, instead of a pair of address counters and a pair of buffer latch units. Thus, Sparr fails to disclose all

limitations of claim 6, and the claim 6 is accordingly patentable.

Regarding dependent claim 7, it is patentable as a matter of law, for at least the following reason it contains all limitations of its patentable base claim 1.

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sparr in view of Christopher.

In response thereto, regarding dependent claim 8, it is patentable as a matter of law, for at least the following reason it contains all limitations of its patentable base clai.

Customer No.: 31561
Docket No.: 13353-US-PA
Application No.: 10/709823

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-4 and 6-9 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Marked Version

INTERFACE AND SYSTEM FOR TRANSMITTING REAL-TIME DATA

BACKGROUND OF THE INVENTION

[0001] Field of the Invention

[0002] The present invention relates to a real-time data transmission interface and a real-time data transmission system, and more particularly, to a real-time data transmission interface and a real-time data transmission system for transmitting a nonreal-time data in real-time and transmitting a real-time data in nonreal-time.

[0003] Description of the Related Art

[0004] A bus composed of a group of conductive wires and used as a communication path, is generally used to transmit data between component and system and between system and system. The conductive wires comprise address lines, data lines, and control lines, which are responsible to transmit the addresses, data, and control signals between component and system, and between system and system during each bus cycle according to the standard of the bus protocol, respectively.

[0005] There are various types of bus in market now, wherein the ANC bus is a military specification high speed/real-time bus, its data transmission rate is up to 4MHz, and it mainly uses 16 bit in parallel for its data transmission. The ANC bus is mainly used to connect a real-time signal processing apparatus, such as a radar system, to a host computer for transmitting a real-time data generated by the real-time signal processing apparatus to the host computer. It is also required by the host computer to transmit the real-time data back to the real-time signal processing apparatus. However, in some cases, the host computer may be a computer which is only capable for nonreal-time data

transmission. For example, a host computer running the operating system such as Microsoft Windows may be used by the radar system to run its self test. When the host computer is a nonreal-time transmission system, the error such as data transmission overtime or data is not transmitted in right order, may be occurred in the real-time signal processing apparatus operation, which causes the real-time signal processing apparatus cannot normally operate.

SUMMARY OF THE INVENTION

[0006] In the light of the preface, it is an object of the present invention to provide a real-time data transmission interface for transmitting the nonreal-time data in real-time and transmitting the real-time data in nonreal-time.

[0007] It is another object of the present invention to provide a real-time data transmission system. The system connects a nonreal-time transmission host computer to a real-time signal processing apparatus, on which the data is transmitted without any error.

[0008] The object of the present invention is to provide a real-time data transmission interface. The interface is suitable for transmitting the nonreal-time data in real-time and transmitting the real-time data in nonreal-time. The real-time data transmission interface provided by the present invention comprises a nonreal-time data interface unit for receiving/transmitting the nonreal-time data, and an I/O unit which is coupled to the nonreal-time data interface unit. Wherein, the I/O unit is used as an interface for transmitting the nonreal-time data and the real-time data. In addition, the present invention further comprises a memory unit and a network interface control unit. The memory unit is coupled to the I/O unit for storing the nonreal-time data and the real-time

data. The network interface control unit is coupled to the memory unit for receiving/transmitting the real-time data.

[0009] In an embodiment of the present invention, the nonreal-time data interface unit comprises a bus interface unit, which is used as an interface for inputting/outputting the nonreal-time data. In addition, the nonreal-time data interface unit further comprises a data output latch, a data input latch, a control signal latch, which are all jointly coupled to the bus interface unit via ~~an~~ a first internal ~~data~~ bus. Moreover, the nonreal-time data interface unit further comprises a buffer and a flag register. Wherein, the buffer is coupled to the bus interface unit via the first internal ~~data~~ bus. The flag register is coupled to the buffer for storing a flag state. Preferably, the nonreal-time data interface unit further comprises a clock generator for generating a clock signal and providing the clock signal to other units, wherein the frequency of the clock signal is 10MHz.

[0010] In addition, the I/O unit comprises a control logic unit, which instructs the I/O unit to perform a read/write operation according to an external control signal. The I/O unit further comprises a checking circuit, a data output latch, and a data input latch, which are all jointly coupled to the control logic unit. Wherein, when a self test mode is activated, the control logic unit controls the checking circuit to check the accuracy of the data output by the I/O unit and to generate a checking result.

[0011] In addition, the memory unit comprises a control logic unit, which controls the memory unit operation according to the external control signal. Moreover, the memory unit further comprises a first address counter, a first memory, and a first buffer latch unit. Wherein, the first address counter is coupled to the control logic unit for providing a first address to the first memory. The first memory is used to store the nonreal-time data, and the first memory is coupled to the first buffer latch unit via a second ~~the~~ internal ~~data~~ bus.

In the embodiment of the present invention, the memory unit further comprises a second address counter, a second memory, and a second buffer latch unit, which are deployed, correspondingly.

[0012] Preferably, the network interface control unit comprises a programmable interface controller and a transistor-transistor logic (hereinafter, referred as TTL)/differential level converting interface. Wherein, the TTL/differential level converting interface is used to convert the type of the real-time data from TTL to differential or in reverse, and to cache the real-time data. In addition, the programmable interface controller comprises a storage apparatus and a sequencer. Wherein, the storage apparatus stores a microcode internally, and the microcode is used to control the operation of the programmable interface controller. The sequencer is coupled to the storage apparatus for ~~running the microcode instructions and~~ adjusting the running order based on an external condition. The programmable interface controller further comprises a condition selector and an event/interrupt handler. Wherein, the condition selector is coupled to the sequencer for caching the external condition, and the external condition is then provided to the sequencer for it to make decision. The event/interrupt handler is coupled to the storage apparatus for processing an interrupt signal or handling an event. In addition, the programmable interface controller further comprises a processor and a parity bit generating/checking apparatus. Wherein, the processor is coupled to the storage apparatus for running the microcode instructions. The parity bit generating/checking apparatus generates a parity bit according to the real-time data provided by the programmable interface controller, and checks the parity bit of the real-time data provided by the programmable interface controller.

File: 13353usf

[0013] According to another aspect of the present invention, the present invention

drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention.

[0016] FIG. 1 is a schematic block diagram illustrating a real-time data transmission system according to a preferred embodiment of the present invention.

[0017] FIG. 2 is a schematic internal block diagram illustrating a real-time data transmission circuit according to a preferred embodiment of the present invention.

[0018] FIG. 3 is a schematic block diagram illustrating the internal configuration of a nonreal-time data interface unit according to a preferred embodiment of the present invention.

[0019] FIG. 4 is a schematic block diagram illustrating the internal configuration of an I/O unit according to a preferred embodiment of the present invention.

[0020] FIG. 5 is a schematic block diagram illustrating the internal configuration of a memory unit according to a preferred embodiment of the present invention.

[0021] FIG. 6 is a schematic block diagram illustrating the internal configuration of a programmable interface controller according to a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] FIG. 1 is a schematic block diagram illustrating a real-time data transmission system according to a preferred embodiment of the present invention. Referring to FIG. 1, the data transmission circuit 200 provided by the present invention for connecting the host computer 110 and the real-time signal processing apparatus 120 works as a real-time data transmission interface. Wherein, the host computer 110 is operated based on a nonreal-time processing operating system, such as Microsoft Windows operating system.

The real-time signal processing apparatus 120, e.g. a radar system, is used to process the real-time signal.

[0023] FIG. 2 is a schematic internal block diagram illustrating a real-time data transmission circuit according to a preferred embodiment of the present invention. Referring to FIG. 2, the real-time data transmission circuit 200 and the host computer 110 transmit the nonreal-time data with each other by using an ISA/PCI bus, for example. In addition, a high speed/real-time data transmission bus, e.g. a military specification ANC bus, is used as a data transmission path between the real-time data transmission circuit 200 and the real-time signal processing apparatus 120 for transmitting data in real time. In the present embodiment, the host computer 110 is coupled to the nonreal-time data interface unit 210 of the data transmission circuit 200 via the ISA/PCI bus in order to provide the nonreal-time data to the data transmission circuit 200. After the nonreal-time data has passed through the I/O unit 220, the nonreal-time data is then stored in the memory unit 230. The real-time signal processing apparatus 120 reads the nonreal-time data stored in the memory unit 230 in real time via the network interface control unit 240. Oppositely, when the real-time signal processing apparatus 120 intends to transmit the real-time data to the host computer 110, the data is transmitted in reverse way.

[0024] To be more specifically, when an application 112 in the host computer 110 knows that the real-time signal processing apparatus 120 requests to transmit data in real time, the application 112 transmits the nonreal-time data as well as a control word "control" which is used to control the memory unit 230 and the network interface control unit 240 to the nonreal-time data interface unit 210 via the ISA/PCI, for example. Then, the nonreal-time data interface unit 210 transmits the nonreal-time data to an I/O port 222 of the I/O unit 220. In addition, the nonreal-time data interface unit 210 stores the control

word "control" to an I/O port 224. Wherein, the I/O port 222 determines whether to write the nonreal-time data into a memory unit 230. If it is determined by the I/O port 222 that it is required to write the nonreal-time data into the memory unit 230, the nonreal-time data is written into the memory (A) 232.

[0025] Referring to FIG. 2 again, after the nonreal-time data has stored in a memory (A) 232, the network interface control unit 240 reads the nonreal-time data from the memory unit 230 in real time according to the control word "control", and transmits the nonreal-time data to the real-time signal processing apparatus 120 via a high speed/real-time data transmission bus, e.g. an ANC bus. Oppositely, when the real-time signal processing apparatus 120 intends to transmit the real-time data to the host computer 110, the real-time data is stored into a memory (B) 234 via the network interface control unit 240. Afterwards, the I/O port 222 reads the real-time data from the memory unit 230, and transmits the real-time data to the host computer 110 in nonreal time via the nonreal-time data interface unit 210.

[0026] The internal configuration of each functional block is described in detail hereinafter, respectively. FIG. 3 is a schematic block diagram illustrating the internal configuration of a nonreal-time data interface unit according to a preferred embodiment of the present invention. As shown in the diagram, an ISA/PCI bus interface unit 301 receives the nonreal-time data transmitted by the ISA/PCI bus first, and then transmits the nonreal-time data to a data output latch 303 and a data input latch 305 via ~~an~~ a first internal ~~data~~ bus 31, respectively. When the nonreal-time data is provided to the nonreal-time data interface unit 210, the nonreal-time data is transmitted to the data output latch 303 via the ISA/PCI bus first, and then transmitted to outside via a data output bus. If it is intended to transmit an external real-time data to the ISA/PCI bus via

the nonreal-time data interface unit 210, the external real-time data is transmitted to the data input latch 305 via an data input bus first, and then transmitted to the ISA/PCI bus interface unit 301 via the first internal ~~data~~ bus, and finally transmitted to outside via the ISA/PCI bus.

[0027] Referring to FIG. 3 again, the ISA/PCI bus interface unit 301 controls the latch/buffer apparatus in other functional block of the present invention, so as to control data transmission direction. In addition, the internal control signal of the nonreal-time data interface unit 210 and the control signal of other functional block of the present invention are cached in a control signal latch 307 via the first internal ~~data~~ bus 31. Then, the control signal for controlling other functional block of the present invention is propagated via a control bus. In addition, a buffer 309 in the nonreal-time data interface unit 210 is coupled to a flag register 311. In the present embodiment, the flag register 311 provides two flags for other functional blocks to setup its flag. An acknowledgement signal "ack" may be used by other functional block of the present invention to setup its flag, and the flag is used to indicate a current state of the functional block. For example, the host computer 110 shown in FIG. 1 can read or clear the flag state stored in the flag register 311 via the first internal ~~data~~ bus 31. When the acknowledgement signal "ack" is enabled, and the host computer 110 has been notified via the ISA/PCI bus interface unit 301 of it, the host computer 110 will read or clear the flag state via the ISA/PCI bus interface unit 301.

[0028] The buffer 309 may be a 3-state (tri-state) buffer, and it is in an "ON" state when the host computer 110 is reading or clearing the flag. When the nonreal-time data interface unit 210 is transmitting data, the buffer 309 is in a high impedance state. In addition, a clock generator 313 may be further included in the nonreal-time data interface

unit 210 for providing an operating clock which is required by the rest of the functional blocks of the present invention. In the present invention, the frequency of the clock signal generated by the clock generator 313 is 10MHz.

[0029] FIG. 4 is a schematic block diagram illustrating the internal configuration of an I/O unit according to a preferred embodiment of the present invention. Referring to FIG. 4, a logic control unit 411 generates and provides an internal control signal to a checking circuit 413, a data output latch 415, and a data input latch 417 according to a control signal which is generated by the nonreal-time data interface unit 210 and transmitted via the control bus. In addition, the logic control unit 411 provides an acknowledgement signal "ack", which is used to indicate the current state of the I/O unit 220. When it is required to transmit the nonreal-time data through the I/O unit 220, the nonreal-time data is transmitted to a bi-directional bus 41 via the data bus first, and then the data output latch 415 extracts the nonreal-time data from the bi-directional bus 41, and determines ~~whether to~~ when to output the nonreal-time data via the data output bus ~~or not~~ according to the control of the control logic unit 411. Oppositely, when it is required to transmit the real-time data via the I/O unit 220, the real-time data is stored into the data input latch 417 via the data input bus first, and then it is determined whether to transmit the real-time data to the bi-directional bus 41 or not according to the control of the control logic unit 411.

[0030] Referring to FIG. 4 again, in the present embodiment, the I/O unit 220 further comprises a checking circuit 413. When the self test mode of the present invention is activated, the checking circuit 413 checks the data output from the I/O unit 220, and provides the checking result to the bi-directional bus 41.

[0031] FIG. 5 is a schematic block diagram illustrating the internal configuration of a memory unit according to a preferred embodiment of the present invention. Referring to

FIG. 5, the memory unit 530 comprises a control logic unit 501 and two sets of symmetric storage modules. Wherein, an address counter (A) 512, a memory (A) 514, and a buffer latch unit (A) 510 togetherly constitute a storage module (A). In addition, an address counter (B) 522, a memory (B) 524, and a buffer latch unit (B) 520 togetherly constitute a storage module (B). Since the operation mode of the storage modules (A) and (B) is rather the same, only the operation principle of the storage module (A) is described in detail hereinafter.

[0032] Referring to FIG. 5 again, the control logic unit 510 is coupled to the address counter (A) 512 and the address counter (B) 522, respectively. In addition, the control logic unit 510 is further coupled to the memory (A) 514 and the memory (B) 524, respectively. Moreover, the control logic unit 501 is coupled to the buffer latch unit (A) 510 and the buffer latch unit (B) 520 via the internal data bus. Wherein, the control logic unit 501 receives an external control signal transmitted by the control bus, so as to generate an internal control signal which is used to control the memory unit 530. The address counter (A) 512 receives an address signal transmitted by the address bus, so as to generate and transmit an address of "address" to the memory (A) 514. The address of the memory (A) 514, i.e. "address", may be either loaded by the host computer 110 shown in FIG. 2 or sequentially generated by the address counter (A) 512. The memory (A) 514 is coupled to the buffer latch unit (A) 510 via <u>a second</u> ~~the internal~~ data bus 51, wherein the buffer latch unit (A) 510 comprises a data input latch (A) 516 and a data output buffer (A) 518. The operating principle and function of the buffer latch unit (A) 510 is similar to the one shown in FIG. 3 and 4, thus its detail description is neglected herein.

[0033] In the present embodiment, the two sets of the storage modules are working independently, thus the two sets of the storage modules can be in the writing state at the

same time. However, since the data output buffer (A) 518 and the data output buffer (B) 528 are sharing a same data output bus, only one storage module is allowed to be in the output state at the same time.

[0034] In addition, the memory unit 230 in the present embodiment further comprises a flag register 503 for providing two flags, which are used by the host computer 110 to configure or clear its value, and the host computer 110 can read the flag state from the flag register 503.

[0035] Referring to FIG. 2 again, the network interface control unit 240 comprises a programmable interface controller 242 and a TTL/differential level converting interface 244. Wherein, the programmable interface controller 242 is responsible for controlling the real-time data transmission of the real-time transmission circuit 200 and the real-time signal processing apparatus 120. The TTL/differential level converting interface 244 is working on a high speed/real-time data transmission bus signal for converting its type from TTL to differential, such that the interference caused by the noise can be avoided.

[0036] FIG. 6 is a schematic block diagram illustrating the internal configuration of a programmable interface controller according to a preferred embodiment of the present invention. Referring to FIG. 6, a microcode is burned into a storage apparatus 601 internally, wherein the microcode is used to control the operation flow of the network interface control unit 240. A sequencer 603 is coupled to the storage apparatus 601 for running the microcode which is burned into the storage apparatus 601. In addition, the sequencer 603 can adjust the running order of the microcode based on an external condition. In the present embodiment, the external condition is generated by a condition selector which is coupled to the sequencer 603. Moreover, the storage apparatus 601 is further coupled to an event/interrupt handler 607 and a microprocessor 609. Wherein, the

event/interrupt handler 607 is used to disable, enable, or handle the interrupt signal or event generated by the host computer of FIG. 2, and the event/interrupt handle 607 can generate and provide an interrupt vector to a condition selector 605, such that the sequencer 603 can run an interrupt service routine.

[0037] The microprocessor 609 is used to run the arithmetic logic unit operations, wherein the operations are instructed by the sequencer 603 for generating a result. In addition, in the present embodiment, the programmable interface controller 242 further comprises a parity bit generating/checking apparatus 611, which is used to check the accuracy of the data parity bit in the programmable interface controller 242, and to generate and provide the parity bit to the data which is output from the programmable interface controller 242.

[0038] In summary, since a parity bit checking/generating apparatus is deployed in the real-time data transmission system of the present invention, the amount of the data transmission error is significantly decreased. In addition, since an address counter is deployed in the memory unit of the present invention, the data sequence error happened in data transmission is also totally eliminated. Furthermore, the real-time data transmission interface provided by the present invention stores the nonreal-time data or real-time data in the memory unit during the data transmission. Therefore, it is possible to transmit the nonreal-time data in real time and transmit the real-time data in nonreal-time.

[0039] Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the

spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.

ABSTRACT OF THE DISCLOSURE

A real-time data transmission interface suitable for transmitting a nonreal-time data in real-time and transmitting a real-time data in nonreal-time is provided. The present invention comprises a nonreal-time data interface unit for receiving/transmitting the nonreal-time data, and an I/O unit which is coupled to the nonreal-time data interface. In addition, the present invention further comprises a memory unit and a network interface control unit. Wherein, the memory unit is used to store the nonreal-time data and the real-time data. The network interface control unit is coupled to the memory unit for receiving/transmitting the real-time data.